

As of 20.05.2024

# **Embedded Multicore Microcontrollers: Practical Application - Face-to-Face Training**

### **Objectives**

This practice-oriented training highlights the key mechanisms and the performance of multicore microcontrollers.

The experience you have gained in numerous practical exercises during the training enables you to master new challenges related to multicore technology efficiently and successfully.

Based on your new know-how, you can efficiently select a multicore  $\mu C$  architecture and estimate the effort and challenges related to a software project.

You can identify problems at an early stage and know how to solve them.

### **Participants**

Developers (software, hardware), software architects, project leaders/managers, system architects

#### Requirements

Basic knowledge of microcontrollers and of C

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### Content

#### **Multicore Microcontroller Architecture**

- Definition of multicore architectures
- Homogeneous/heterogeneous multicore architectures with shared memory and/or non-shared memory
- Software aspects for multicore processing
- Core interfaces and memories: core-local cache and SPRAM (level 1 memory); global/shared SRAM (level 2 memory), snoop logic, cache coherency
  - Requirements for instruction throughput (MIPS)
- Core synchronization
- Co-processor functionality
- New core bus systems (crossbar)
- Semaphores: memory resource access control
- Memory protection (access protection)
- Multicore interrupt processing
- Multicore start-up/initialization: boot process, set-up of primary and secondary CPU(s)
- Debug interface(s)

# **Multicore Microcontroller Tool Aspects**

- C/C++ compiler: extensions for multicore
- Locating program and data sections in specific memory areas/segments; control of access rights to global/external definitions
- Locator safety support: variable access control for multicore modules

### **RTOS**

- Multicore aspects for RTOS software
- Scheduler: software/task deployment and execution strategies
- Partitioning
- Task synchronization concepts
- Task communication concepts
- Programming models and multicore API: communication, resource management

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- Examples of multicore RTOS implementations

#### **Multicore Debugging and Test Aspects**

- Debugger extensions for multicore: core synchronization during debugging, synchronous start/stop, multicore breakpoint handling, core context sensitive visualization
- Performance and timing analysis, analysis of software runtime behaviour (profiling)
- Multicore and trace handling

#### Safety

- Multicore in standards
- Hardware safety measures
- Safety management unit SMU
- Bus error detection and protection mechanisms
- Safety core (checker core, lockstep core)
- Safety on-chip test features

### Practical Exercises - Performed on an Evaluation Board based on Aurix Microcontrollers

- Multicore start-up behavior
- Memory allocation and partitioning
- Decomposition of existing singlecore applications
- Porting to multicore
- Synchronization/communication
- Protection mechanisms
- Performance measurement

#### **FACE-TO-FACE TRAINING**

DatePrice \*Duration24.07.2024 - 26.07.2024 2.100,00 €3 days05.03.2025 - 07.03.2025 2.100,00 €3 days

Training code: E-µCMULTI

## Live Online - English

**Date Duration** 16.10. – 18.10.20243 days

### Face-To-Face - German

**Date Duration** 24.07. – 26.07.20243 days 05.03. – 07.03.20253 days

# **Live Online - German**

**Date Duration** 16.10. – 18.10.20243 days

## Coaching

Our coaching services offer a major advantage: our specialists introduce their expertise and experience directly in your solution process, thus contributing to the success of your projects.

We will be happy to provide you with further information or submit a quotation tailored to your requirements.

<sup>\*</sup> Price per attendee, in Euro plus VAT